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GTLP8T306
8-Bit LVTTL/GTLP Bus Transceiver

General Description

The GTLP8T306 is an 8-bit bus transceiver that provides LVTTL to GTLP signal level translation. The device provides a high speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal output edge-rate control and is process, voltage, and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver thresholds. The GTLP output LOW level is typically less than 0.5V, the output HIGH level is 1.5V and the receiver threshold is 1.0V.

Features

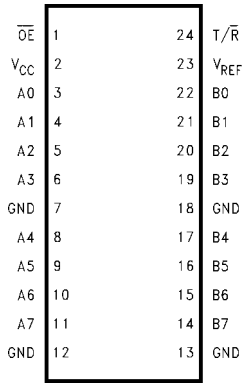
- Bidirectional interface between GTLP and LVTTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced CMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- 5V over voltage tolerance on LVTTL ports
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- A Port source/sink –24mA/+24mA
- B Port sink +50mA

Ordering Code:

Order Number	Package Number	Package Description
GTLP8T306MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A0–A7	Side A Inputs or 3-STATE Outputs
B0–B7	Side B Inputs or 3-STATE Outputs
V_{REF}	GTLP Reference Voltage

Truth Table

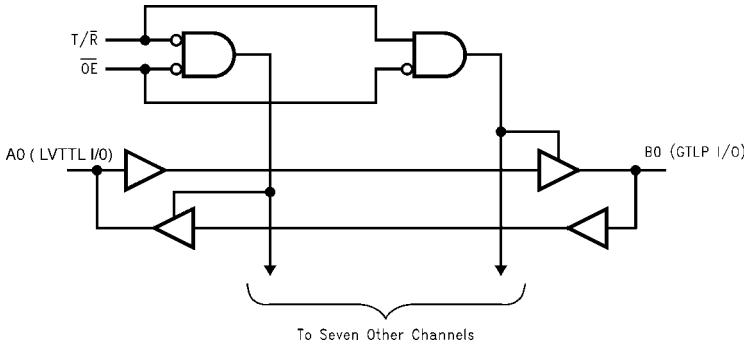
Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
H	X	HIGH Z on Bus A and Bus B
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B

Functional Description

The GTLP8T306 is an 8-bit transceiver providing the standard 245 functionality that supports both GTL and GTLP signal levels.

Data polarity is non-inverting and the data flow direction is controlled by the T/$\overline{R}$ pin. The outputs are enabled to allow data through the device when $\overline{OE}$ is LOW otherwise both the A and B ports are placed in a HIGH impedance state.

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to 7.0V
DC Output Sink Current into A-Port, I_{OL}	48 mA
DC Output Source Current from	
A Port I_{OH}	−48 mA
DC Output Sink Current into B-Port	
in the LOW State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
$V_O > V_{CC}$	+50 mA
ESD Rating	>2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Supply Voltage V_{CC}	3.15V to 3.45V
Bus Termination Voltage (V_{TT})	
GTLP	1.35V to 1.65V
GTL	1.14V to 1.26V
Input Voltage (V_I) on A-Port	
and control pins	0V to 5.5V
HIGH Level Output Current (I_{OH})	
A Port	−24 mA
LOW Level Output Current (I_{OL})	
A Port	+24 mA
B Port	+50 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
V_{IH}	B Port			V_{REF} +0.05		V_{TT}	V
	Others			2.0			V
V_{IL}	B Port			0.0		V_{REF} −0.05	V
	Others					0.8	V
V_{REF}	GTLP				1.0		V
	GTL				0.8		V
V_{IK}		V_{CC} = 3.15V	I_I = −18 mA			−1.2	V
V_{OH}	A Port	V_{CC} = Min to Max (Note 5)	I_{OH} = −100 µA	V_{CC} −0.2			V
		V_{CC} = 3.15V	I_{OH} = −12 mA	2.4			
			I_{OH} = −24 mA	2.0			
V_{OL}	A Port	V_{CC} = Min to Max (Note 5)	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15V	I_{OL} = 24 mA			0.5	
	B Port	V_{CC} = 3.15V	I_{OL} = 40 mA			0.4	V
			I_{OL} = 50 mA			0.55	
I_I	A Port	V_{CC} = 3.45V	V_I = 5.5V			20	µA
			V_I = 0V			−20	
	Control Pins	V_{CC} = 3.45V	V_I = 5.5V			5	µA
			V_I = 0V			−5	
	B Port	V_{CC} = 3.45V	$V_I = V_{TT}$			5	µA
			V_I = 0			−5	
I_{OFF}	A Port	V_{CC} = 0	V_I or V_O = 0 to 4.5V			100	µA
I_I (Hold)	A Port	V_{CC} = 3.15V	V_I = 0.8V	75			µA
			V_I = 2.0V	−20			
I_{OZH}	A Port	V_{CC} = 3.45V	V_O = 3.45V			20	µA
	B Port		V_O = 1.5V			5	
I_{OZL}	A Port	V_{CC} = 3.45V	V_O = 0			−20	µA
	B Port	V_{CC} = 3.45V	V_O = 0.55			−5	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 4)	Max	Units
I_{CC}	A or B Ports	V_{CC} = 3.45V	Outputs HIGH		7	18	mA
		I_O = 0	Outputs LOW		8	20	
		$V_I = V_{CC}$ or GND	Outputs Disabled		8	20	
I_{CC} (Note 6)	A Port and Control Pins	V_{CC} = 3.45V, A or Control Inputs at V_{CC} or GND	One Input at V_{CC}–0.6V		0	1	mA
C_{IN}	Control Pins		$V_I = V_{CC}$ or 0		5		pF
	A Port		$V_I = V_{CC}$ or 0		7		
	B Port		$V_I = V_{CC}$ or 0		9		

Note 4: All typical values are V_{CC} = 3.3V and T_A = 25°C.

Note 5: For conditions shown as Min, use the appropriate value specified under recommended operating conditions.

Note 6: This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air-temperature, V_{REF} = 1.0V (unless otherwise noted).

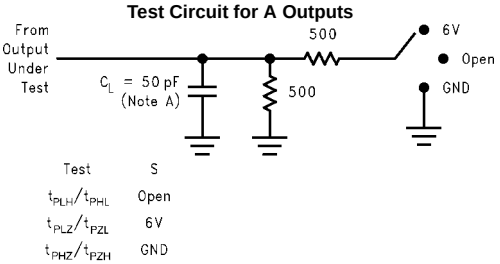
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 7)	Max	Units
t_{PLH}	An	Bn	1.0	4.0	7.5	ns
t_{PHL}			1.0	5.1	7.5	
t_{PLH}	Bn	An	1.0	5.8	8.3	ns
t_{PHL}			1.0	4.9	8.3	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			2.6		ns
t_{FALL}	Transition Time, B Outputs (20% to 80%)			2.6		ns
t_{RISE}	Transition Time, A Outputs (10% to 90%)			2.5		ns
t_{FALL}	Transition Time, A Outputs (10% to 90%)			2.5		ns
t_{PZH}, t_{PZL}	$\overline{OE}$	An	1.0	4.5	9.5	ns
t_{PHZ}, t_{PLZ}			1.0	4.9	9.5	
t_{PLH}	$\overline{OE}$	Bn	1.0	5.4	9.5	ns
t_{PHL}			1.0	6.0	9.5	

Note 7: All typical values are at V_{CC} = 3.3V and T_A = 25°C.

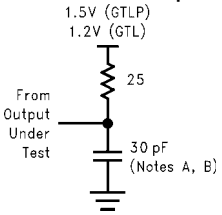
Test Circuit and Timing Waveforms

Test Circuit for A Outputs

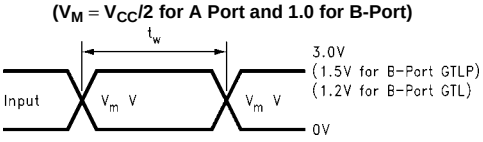


Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

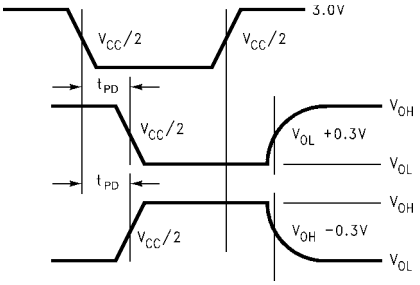
Test Circuit for B Outputs



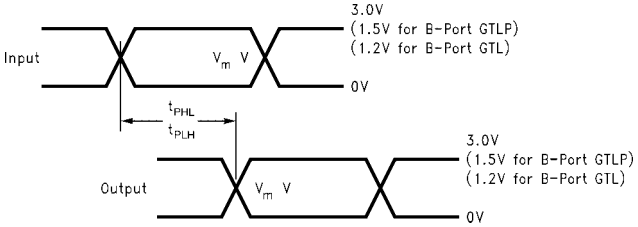
Voltage Waveforms Pulse Duration
($V_M = V_{CC}/2$ for A Port and 1.0 for B-Port)



Voltage Waveforms Enable and Disable Times A Port



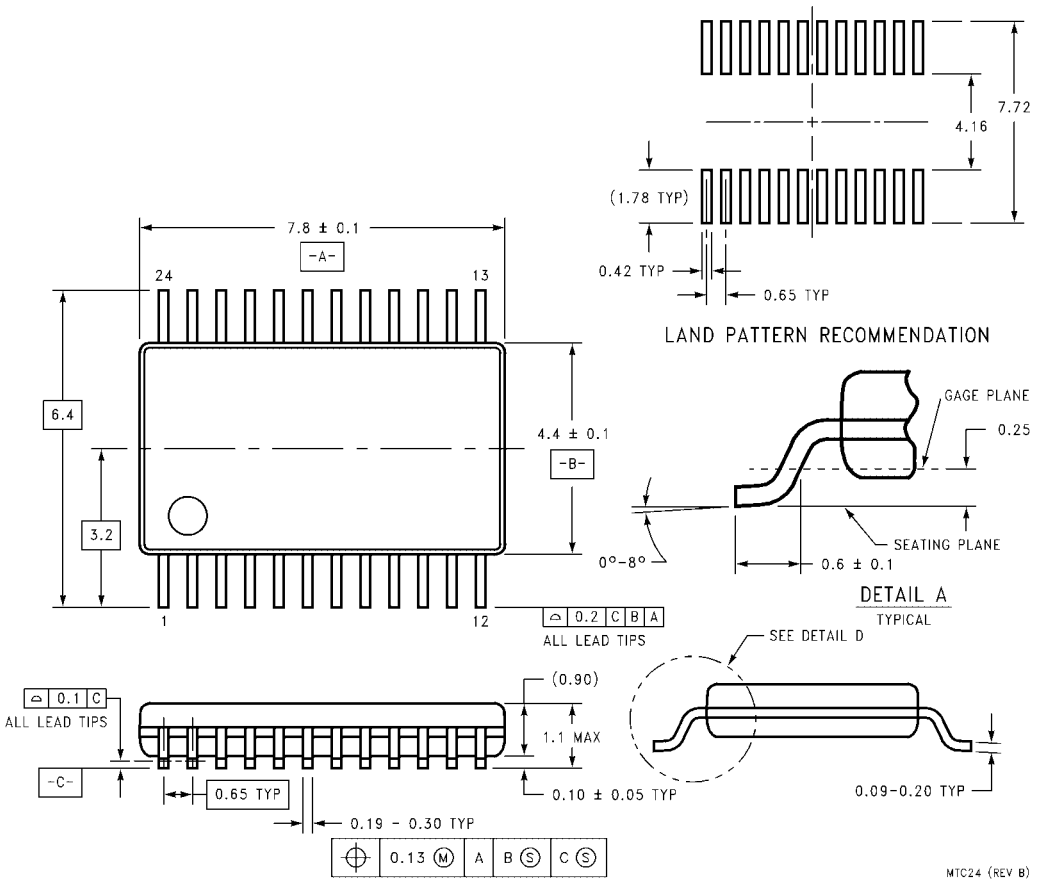
Voltage Waveforms Propagation Delay and Setup and Hold Times
($V_M = V_{CC}/2$ for A Port and 1.0 for B Port)



Note A: C_L includes probes and Jig capacitance.

Note B: For B Port, C_L = 30 pF is used for worst case.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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